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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,195	12/21/2000	Toshiyuki Hirota	040373/0300	7014

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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/741,195	HIROTA ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-9,11-16 and 18-23* is/are pending in the application.

4a) Of the above claim(s) *5,10,17,24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9,11-16 and 18-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Applicant's election of group II, claims 1-4, 6-9, 11-16 and 18-21, 22-23 in Paper No. 4 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Applicant's election without traverse of group II, claims 1-4, 6-9, 11-16 and 18-21, 22-23 in Paper No. 4 is acknowledged.

Claims 5, 10, 17 and 24 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 4.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: the reference number 123a (page 5, line 25) is not on the figure. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because there are more than 150 words.

Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 – 4, 6 – 9, 11 – 16, 18 – 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,251,721 to Kanazawa et al.

Regarding claims 1 and 6, Kanazawa et al. teach a method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film (5) on a surface of the semiconductor substrate;

forming gate electrodes (7) on a surface of the gate oxide film, and forming nitride protective films (31) on the gate electrodes;

uniformly forming a first nitride film (10) having a predetermined thickness on the surface with the gate electrodes formed thereon;

uniformly forming a second nitride film (15) having a predetermined thickness on the surface on which the first nitride film is etched;

self-aligning the high-density region using the first nitride film positioned on sides of the gate electrodes as an etching stopper to form contact holes reaching the semiconductor substrate in the interlayer insulating film;

forming contact electrodes connected to the semiconductor substrate in the contact holes (see figures 1 A – C; 2 A – B; column 6, line 12 – column 7, line 61).

Kanazawa et al. do not teach a method of forming oxide films on the gate electrodes. It would have been a matter of obvious design choice to select an oxide for the protective cap layer on the gate electrode since it is a known material that is well suited for the intended use.

Kanazawa et al. do not teach a method of etching the first nitride film in only the low-density region to expose the gate oxide film in gaps between the gate electrodes. The gate oxide in the gap between the gate stacks has no effect on the operation of the device. Therefore, it would have been a matter of obvious design choice to etch only to the surface or to remove it.

Kanazawa et al. teach a method of forming an interlayer insulating film on the second nitride. Kanazawa et al. do not teach a forming an interlayer insulating film with an impurity introduced therein on a surface of the second nitride film. Impurity containing interlayer

insulating films such as BPSG are known in the art, and it would have been obvious to select such a material since it is well suited for the intended use. Additionally, it is desirable to use certain impurity containing dielectric films for interlayer insulators since they often have low dielectric constants, which reduce the capacitance of interconnect structures.

Kanazawa et al. do not teach each anneal step as cited in the claimed invention. It is common in the art to perform annealing steps to repair substrate damage, activate dopants, form silicide and other reasons. It would have been a matter of obvious design choice to perform annealing steps at any time during fabrication.

Regarding claims 2, 7, 12 and 19, Kanazawa et al. teach a method, wherein the second nitride film is formed by a chemical vapor deposition process. Kanazawa et al. do not teach the first nitride film is formed by a CVD. Kanazawa et al. is silent with respect to how the first nitride film is deposited. One having ordinary skill in the art would have been required to select a known method of deposition. It would have been obvious to select CVD, as a mater of design choice since it is a well known method.

Regarding claims 3, 8, 13, 20, 15 and 22, Kanazawa et al. teach a method, wherein the first and second nitride films are formed to a thickness of about 30nm. Kanazawa et al. do not teach a method, wherein the second nitride film is formed to a thickness ranging from 3.0 to 20 nm. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to have a thickness ranging from 3.0 to 20 nm for second nitride as a matter of obvious design choice, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art.

Regarding claims 4, 9, 16 and 23, Kanazawa et al. teach a method, wherein the first nitride film is formed to a thickness large enough to serve as an etching stopper for self-aligning the high-density region. Kanazawa et al. do not explicitly teach the second nitride film is formed to a thickness which prevents an impurity of the interlayer insulating film from being diffused into the semiconductor substrate by annealing the assembly in the atmosphere containing the water vapor and also prevents the semiconductor substrate from being oxidized by annealing the assembly in the atmosphere containing the water vapor, but allow the forming gas to be diffused into the semiconductor substrate. It would have been a matter of obviousness for one having ordinary skill in the art to have arrived at an optimal thickness of the second nitride film, as explained in the above paragraph.

Regarding claims 11 and 18, Kanazawa et al. teach a method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of the semiconductor substrate;

forming gate electrodes on a surface of the gate oxide film, and forming nitride protective films on the gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

etching the first nitride film and gate oxide to expose the substrate in gaps between gate electrodes in said in the low-density region;

uniformly forming a second nitride film having a predetermined thickness on the surface on which the first nitride film is etched;

self-aligning the high-density region using the first nitride film positioned on sides of the gate electrodes as an etching stopper to form contact holes reaching the semiconductor substrate in the interlayer insulating film;

forming contact electrodes connected to the semiconductor substrate in the contact holes. (see figures 1 A – C; 2 A – B; column 6, line 12 – column 7, line 61).

Kanazawa et al. do not teach a method of forming oxide films on the gate electrodes. It would have been a matter of obvious design choice to select an oxide for the protective cap layer on the gate electrode since it is a known material that is well suited for the intended use.

Kanazawa et al. do not explicitly teach a method of etching the first nitride film in only the low-density region to expose the gate oxide film in gaps between the gate electrodes and then removing the gate oxide film in a separate step. Since the etch rates of the gate oxide layer and first nitride film are different, one of ordinary skill in the art would have been required to remove the layers in two etch steps.

Kanazawa et al. teach a method of forming an interlayer insulating film on the second nitride. Kanazawa et al. do not teach a forming an interlayer insulating film with an impurity introduced therein on a surface of the second nitride film. Impurity containing interlayer insulating films such as BPSG are known in the art, and it would have been obvious to select such a material since it is well suited for the intended use. Additionally, it is desirable to use certain impurity containing dielectric films for interlayer insulators since they often have low dielectric constant, which reduce the capacitance of interconnect structures.

Kanazawa et al. do not teach each anneal step as cited in the claimed invention. It is common in the art to perform annealing steps to repair substrate damage, activate dopants, form silicide and other reasons. It would have been a matter of obvious design choice to perform annealing steps at any time during fabrication.

Regarding claims 14 and 21, Kanazawa et al. do not teach a method, wherein the first nitride film is formed by a chemical vapor deposition process, and the second nitride film is formed by a rapid thermal nitriding process. Kanazawa et al. is silent with respect to how the first nitride film is deposited. It would have been obvious to select CVD, as a mater of design choice since it is a well known method. Rapid thermal nitriding is a well known a method of forming nitride layer. It would have been a matter of obvious design choice to select it.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QVU
February 11, 2002

Steven Loke
Primary Examiner

Steven Loke